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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,373	01/17/2002	Ernst Bretschneider	DE 010005	3917

24738 7590 11/23/2005

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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EXAMINER	
REIS, TRAVIS M	

ART UNIT	PAPER NUMBER
2859	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,373	BRETSCHNEIDER ET AL.	
	Examiner	Art Unit	
	Travis M. Reis	2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11,13-17,19-27 and 29-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11,13-17,19-27 and 29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 2, 4-17, & 19-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrenk (U.S. Patent 4910707) in view of Berger et al. (U.S. Patent 5225706) & Hayami et al. (U.S. Patent 6426495).

Schrenk discloses an electric circuit arrangement for protecting a chip arrangement comprising a optosensitive detector unit (8) arranged underneath a dielectric opaque epoxy insulation oxide layer with a plurality of pnp photodiodes (col. 4 lines 5-15) (Figure 4), a power supply resistor (15) & a reference resistor (16); whose output voltage is a measure of the intensity of incident light on the detector unit, an evaluation/logic unit/logic gates unit, connected to the sensor outputs and blocking circuits (10a)(col. 2 lines 11-17); and connected to an erasable EEPROM storage unit (5) further connected to a control logic unit (7); wherein the data of the chip arrangement to be protected can be permanently blocked, or short circuited (1a)

(col. 1 lines 61-68) (col. 2 lines 52-58).

Schrenk does not disclose a comparator unit preceded by the detector unit provided for comparing the output voltage of the detector unit with an adjustable reference voltage or the generation of a failure message occurring during comparison of the output voltage of the detector unit with the reference voltage when the output voltage deviates from the nominal range.

Hayami et al. discloses temperature compensating circuit, temperature compensating logarithm conversion circuit and light receiver (Figure 1) with a comparator unit (col. 17 line 29) provided for comparing the output voltage of the detector unit (col. 17 line 23) with an adjustable working point/monitor signal (i.e. "freely set detection level") (col. 17 lines 27-28) which then generates a failure message (col. 17 lines 30-33) when the output voltage deviates from the nominal range (col. 17 lines 26-35) in order to sense failure before it occurs (col. 17 lines 29-30). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the comparator unit disclosed by Hayami et al. to the detector unit disclosed by Schrenk in order to improve the reaction time of the detector unit to protect the data by blocking or short circuit.

Furthermore, with reference to claims 17 & 18, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed (i.e. implemented and/or integrated in a card) does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. ***Ex parte Masham***, 2 USPQ2d 1647 (1987).

Schrenk does not disclose a bipolar transistor with emitter connected to the input of the comparator unit and the power supply voltage via the power supply resistor, while a collector is connected to ground via the reference resistor, and a junction of the bipolar transistor is

provided for absorbing light; wherein at least one bipolar transistor is disposed in a plane of the data or functions to be protected; but does disclose that photoresistors are also suitable sensors (col. 3 line 37)

Berger et al. discloses a matrix of photosensitive elements associating a photodiode or a phototransistor (aka bipolar resistor) (i.e. that a photodiode is replaceable with a phototransistor) and a storage capacitor with an emitter (38), a junction (36) for absorbing light, and collector (34) (Figure 5) (col. 7 lines 7-25) wherein the bipolar transistor is in a vertical plane with the data to be protected, wherein the phototransistor has the advantage of a higher sensitivity (col. 1 lines 28-31). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to replace the photodiode disclosed by Schrenk with the phototransistor, emitter & collector disclosed by Berger et al. and to connect them to the power supply resistor & reference resistor disclosed by Schrenk in order that the device would have the advantage of a higher sensitivity.

Response to Arguments

4. In response to applicant's arguments that none of the cited references provide the limitation "working point of the detector unit or a threshold value of the reference voltage is adjustable"; these arguments have been fully considered but they are not persuasive since the monitor signal disclosed by Hayami et al. is "freely set", as detailed above in paragraph 3.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Travis M. Reis whose telephone number is (571) 272-2249. The examiner can normally be reached on 8--5 M--F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Travis M Reis
Examiner
Art Unit 2859

Diego Gutierrez
Supervisory Patent Examiner
Tech Center 2800

tmr
November 21, 2005